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	Document ID	Kind Codes	Source	Issue Date	P
2	US 20040085831		US-PGPU	20040506	27
3	US 20040047214		US-PGPU	20040311	14
4	US 20030174539		US-PGPU	20030918	12
5	US 20030117856		US-PGPU	20030626	38
6	US 20030072175		US-PGPU	20030417	27
7	US 20030026145		US-PGPU	20030206	18
8	US 20030026144		US-PGPU	20030206	18
9	US 20030021172		US-PGPU	20030130	28
10	US 20030021154		US-PGPU	20030130	18
11	US 20030016560		US-PGPU	20030123	20
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14	US 20020075727		US-PGPU	20020620	12
15	US 20010014037		US-PGPU	20010816	9
16	US 6717861 B2		USPAT	20040406	13
17	US 6704239 B2		USPAT	20040309	26
18	US 6552950 B2		USPAT	20030422	16
19	US 6480419 B2		USPAT	20021112	16
20	US 6335881 B1		USPAT	20020101	10
21	US 6304486 B1		USPAT	20011016	16
22	US 6288936 B1		USPAT	20010911	27
23	US 6278636 B1		USPAT	20010821	11
24	US 6067248 A		USPAT	20000523	14
25	US 5996041 A		USPAT	19991130	14
26	US 5982663 A		USPAT	19991109	20
27	US 5768215 A		USPAT	19980616	22
28	US 5761132 A		USPAT	19980602	9
29	US 5748531 A		USPAT	19980505	13
30	US 5748529 A		USPAT	19980505	9
31	US 5677873 A		USPAT	19971014	7
32	US 5448578 A		USPAT	19950905	13

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(54) NONVOLATILE MEMORY FOR STORING MULTIVALUE DATA

(75) Inventor: Shokki Kawamura, Kawasaki (JP)

(73) Assignee: Fujitsu Limited, Kawasaki (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/734,233

(22) Filed: Dec. 12, 2000

(30) Foreign Application Priority Data

Jan. 30, 2000 (JP) 12-199601

(51) Int. Cl.[7] G11C 16/04

(52) U.S. Cl. 365/185.03; 365/185.24; 365/185.28; 365/185.05

(58) Field of Search 365/185.03, 185.24, 365/185.28, 185.05, 185.01, 185.21, 185.22, 185.18

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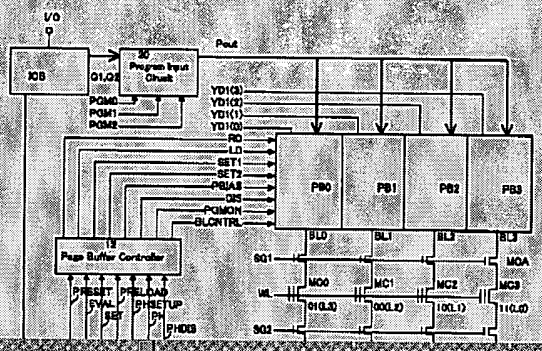
Primary Examiner—David Nelms
Assistant Examiner—David Lam
(74) *Attorney, Agent, or Firm*—Arent Fox Kintner Plotkin & Kahn, PLLC

(57) ABSTRACT

A nonvolatile memory that has a plurality of floating gate type cell transistors comprises a read buffer circuit, connected to the bit line, that detects the threshold voltage states in the cell transistor. Each cell transistor can hold 2^N threshold voltage states and accordingly, the read buffer circuit reads N bits of data. For this purpose, the read buffer circuit has a latch circuit that latches the read data in accordance with the detected threshold voltage state. This latch circuit has a first and second latch reversal circuit for reversing the latched state to the first or second state. When the read buffer circuit reads the first bit being held in the cell transistor, the latch circuit in its initial state is reversed or not reversed by the first latch reversal circuit in accordance with the detected first and second threshold voltage state, or third and fourth threshold voltage state, and that latch state is output as the first data. Furthermore, when the lower order second bit held in the cell transistor is read next, the read buffer circuit is reversed or not reversed from the latch state corresponding to the first data above by the first latch reversal circuit in accordance with the detected first or second threshold voltage state. Then, it is reversed or not reversed by the second latch reversal circuit in accordance with the detected third or fourth threshold voltage state and the latch state is output as the second data.

11 Claims, 18 Drawing Sheets



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	Document ID	Kind Codes	Source	Issue Date	R
2	US 20040085831		US-PGPU	20040506	27
3	US 20040047214		US-PGPU	20040311	14
4	US 20030174539		US-PGPU	20030918	12
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17	US 6704239 B2		USPAT	20040309	26
18	US 6552950 B2		USPAT	20030422	16
19	US 6480419 B2		USPAT	20021112	16
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22	US 6288936 B1		USPAT	20010911	27
23	US 6278636 B1		USPAT	20010821	11
24	US 6067248 A		USPAT	20000523	14
25	US 5996041 A		USPAT	19991130	14
26	US 5982663 A		USPAT	19991109	20
27	US 5768215 A		USPAT	19980616	22
28	US 5761132 A		USPAT	19980602	9
29	US 5748531 A		USPAT	19980505	13
30	US 5748529 A		USPAT	19980505	9
31	US 5677873 A		USPAT	19971014	7
32	US 5448578 A		USPAT	19950905	13

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HAVING INTERLEAVED READ CAPABILITY AND METHODS OF OPERATING SAME

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[73] Assignee: **Samsung Electronics Co., Ltd.**, Suwon, Rep. of Korea

[21] Appl. No.: 722,478

[22] Filed: Sep. 27, 1996

[30] **Foreign Application Priority Data**

Sep. 28, 1995 [KR] Rep. of Korea 1995-32483

[51] Int. Cl.[6] G11C 8/00

[52] U.S. Cl. 365/238.5; 365/185.12; 365/189.05; 365/239

[58] Field of Search 365/238.5, 185.11, 365/185.12, 189.05, 239

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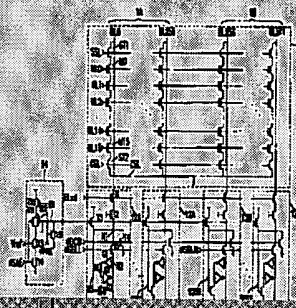
Primary Examiner—Huan Hoang
Attorney, Agent, or Firm—Myers Bigel Sibley & Sajovec

[57] **ABSTRACT**

Integrated circuit memory devices having interleaved read capability include read controllers and subpage data buffers for performing interleaved read operations. These read operations are performed by downloading respective subpages of memory while simultaneously serially transmitting previously downloaded subpages of memory so that consecutive pages of memory data can be serially transmitted as a continuous string of data without the occurrence of breaks therebetween caused by stand-by holding periods. These memory devices typically contain an array of memory cells arranged as a plurality of pages (e.g., rows) of predetermined width coupled to a respective plurality of word lines and a plurality of columns of memory cells electrically coupled to a respective plurality of bit lines. First and second subpage buffers may also be provided for temporarily storing subpages of data read from addressed subpages of memory cells. The read controller is also provided for initiating transfer of a previously read subpage of data from one of the first or second subpage buffers to an I/O data buffer, while simultaneously initiating an interleaved page read operation to read another subpage of data from memory into the other of the first or second subpage buffers. The interleaved page read operation is preferably performed to prevent the occurrence of breaks in the transfer of data to the I/O data buffer when multiple pages of data are being downloaded and serially transmitted to external the memory device.

12 Claims, 11 Drawing Sheets



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